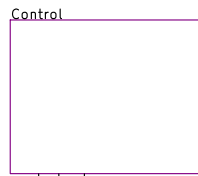


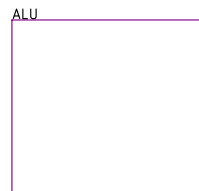
clock.sch



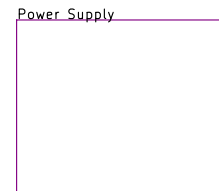
state.sch



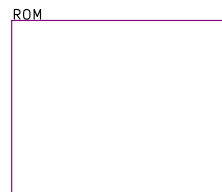
control.sch



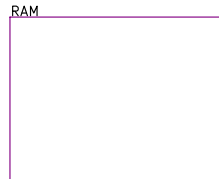
alu.sch



power.sch



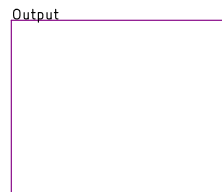
rom.sch



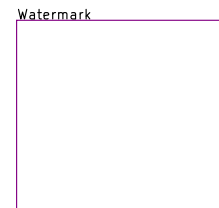
ram.sch



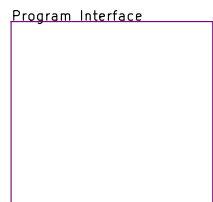
label.sch



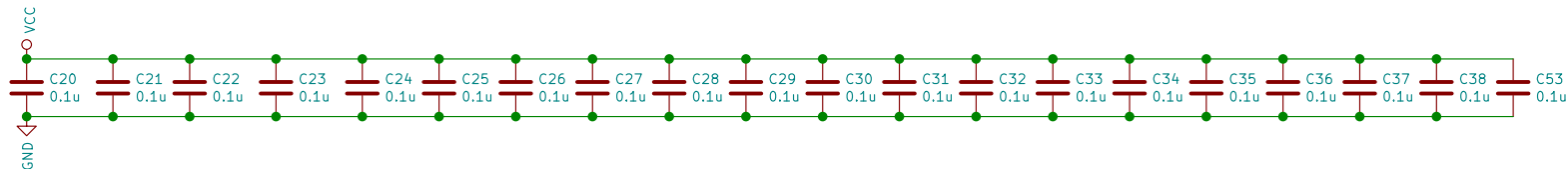
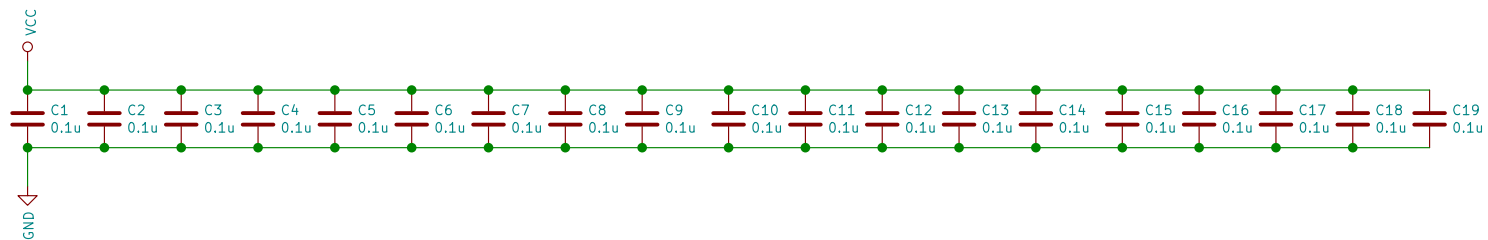
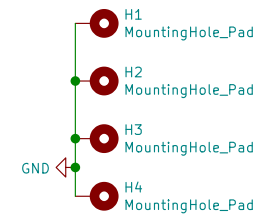
output.sch



watermark.sch



program.sch



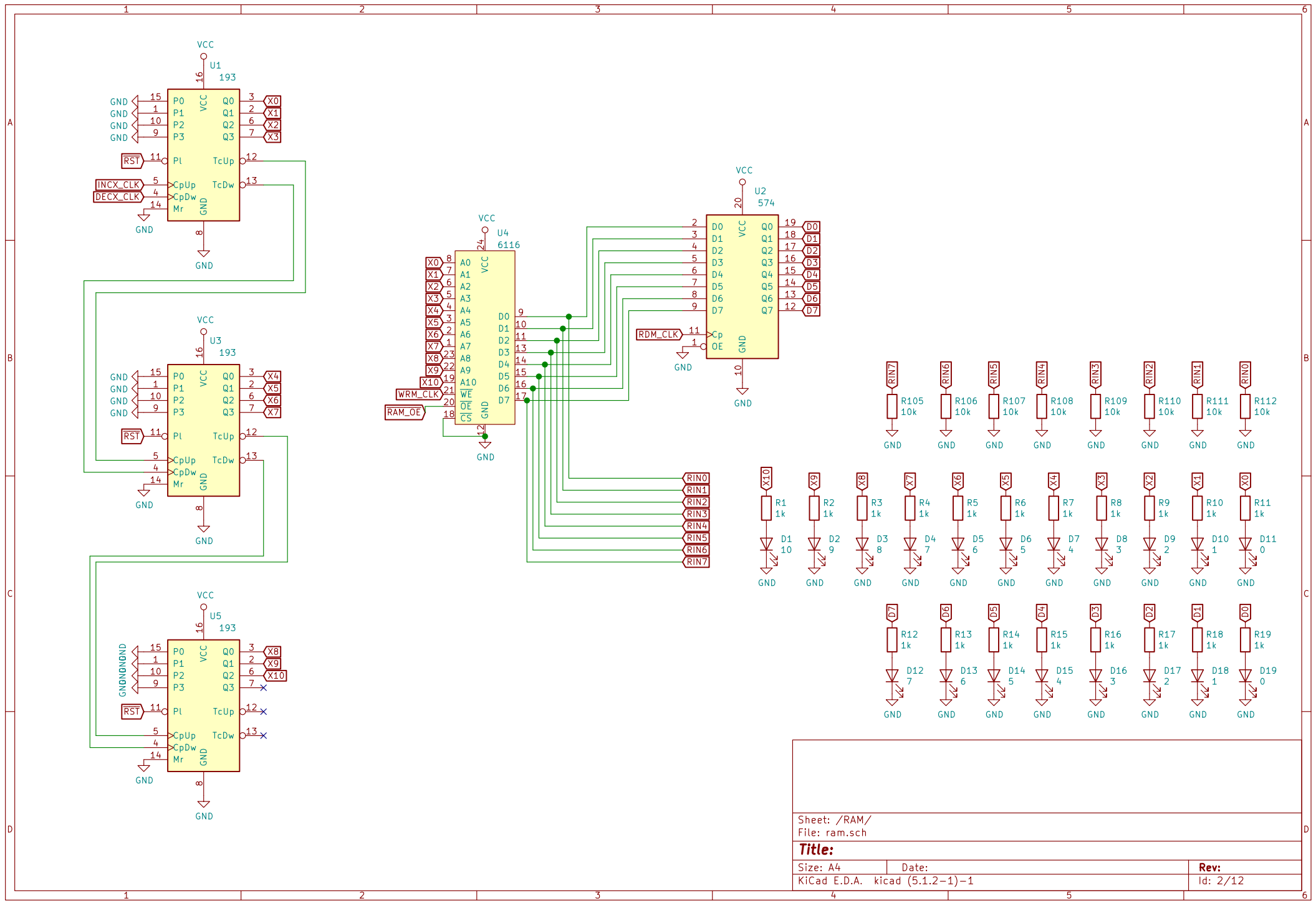
Sheet: /  
File: bfp.sch

**Title:**

Size: A4  
KiCad E.D.A. kicad (5.1.2-1)-1

Date:

**Rev:**  
Id: 1/12



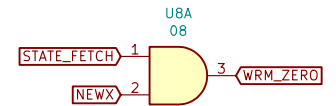
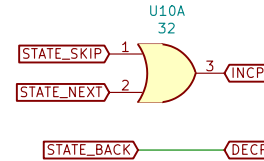
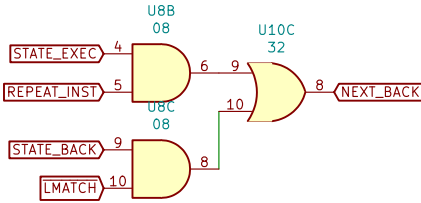
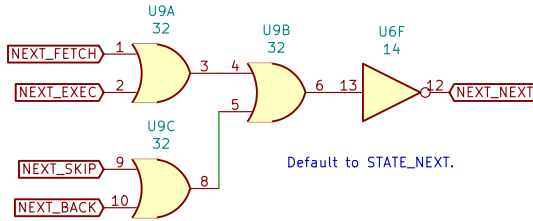
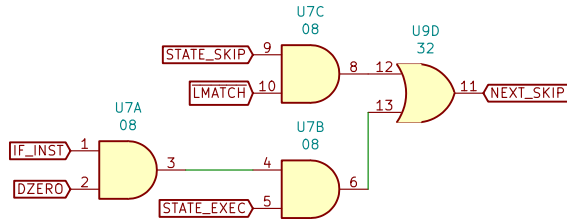
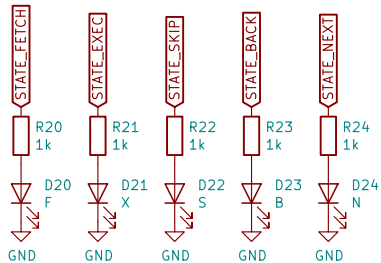
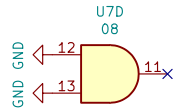
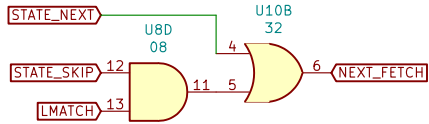
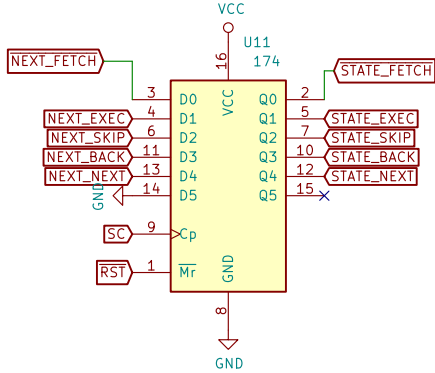
Sheet: /RAM/  
 File: ram.sch

**Title:**

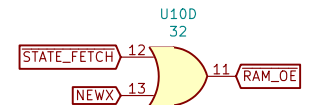
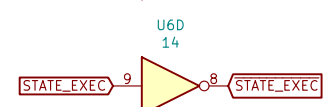
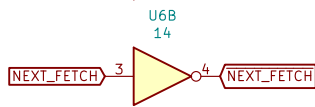
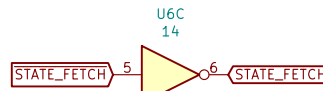
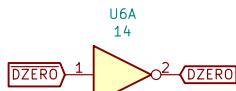
Size: A4	Date:
KiCad E.D.A. kicad (5.1.2-1)-1	Rev: Id: 2/12

The states are:  
 FETCH - Fetch cell from RAM (or clear cell).  
 EXEC - Execute the instruction (possibly writing a cell).  
 SKIP - Skip to the matching '['.  
 BACK - Go back to the matching '].'  
 NEXT - Increment P.

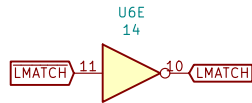
Since we start in STATE\_NEXT, we store the inverted value so it resets to being set.



If we're in STATE\_FETCH and hit a new watermark (NEWX), we write a zero.



We read from RAM only in STATE\_FETCH, and only if we haven't hit a new watermark (NEWX).



State machine and next state logic.  
 This schematic includes some control logic as well to make it fit in fewer ICs.

Sheet: /State/  
 File: state.sch

**Title:**

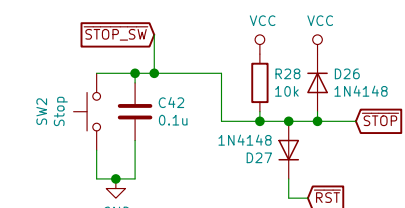
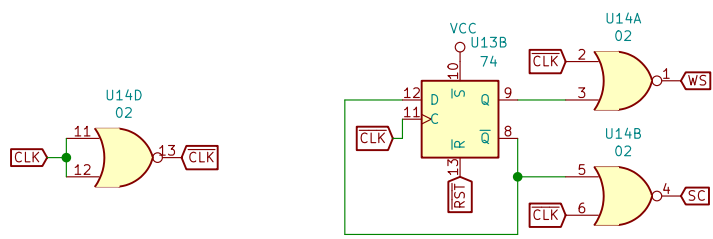
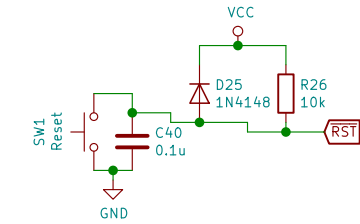
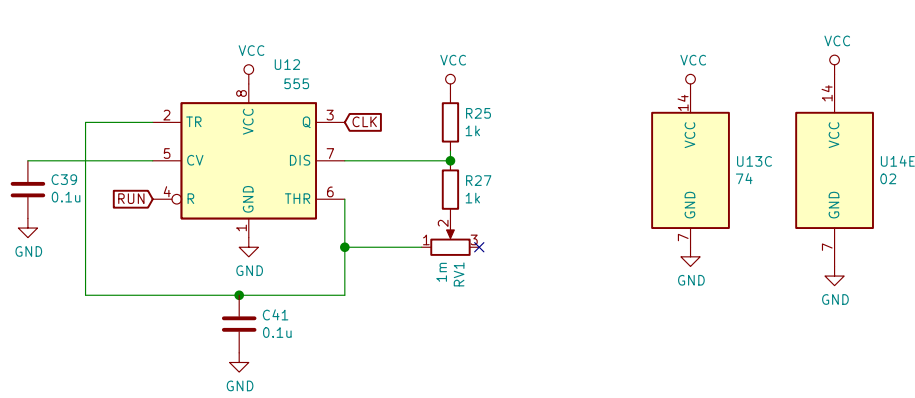
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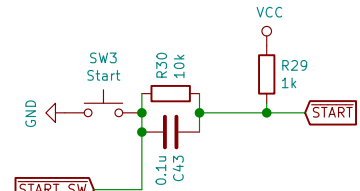
**Rev:**

KiCad E.D.A. kicad (5.1.2-1)-1

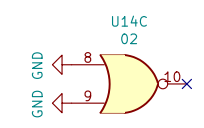
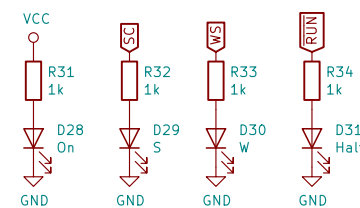
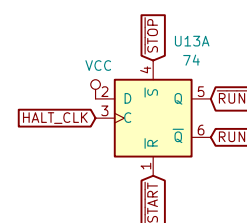
Id: 3/12



Stop the clock.  
Note that we stop the clock on reset too.

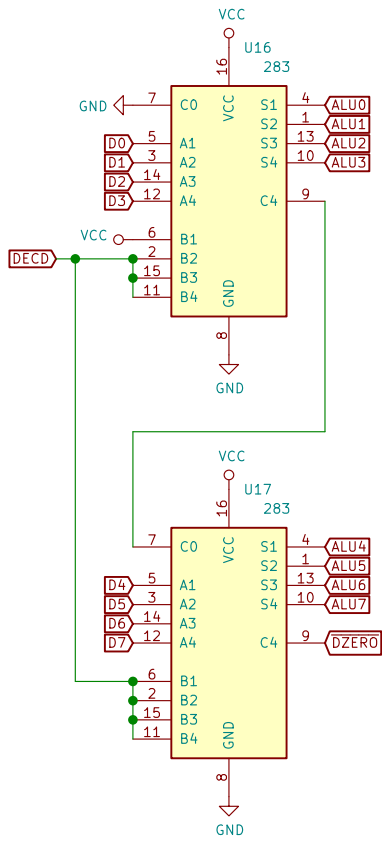


Start the clock.

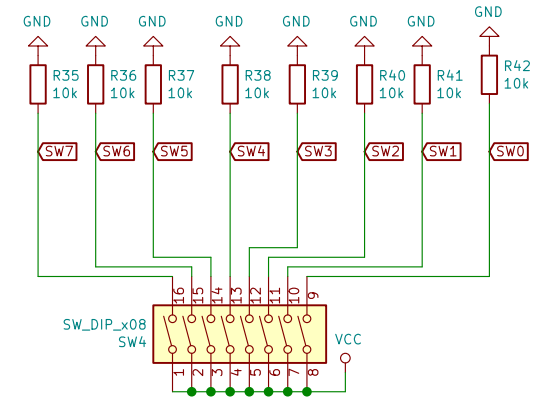
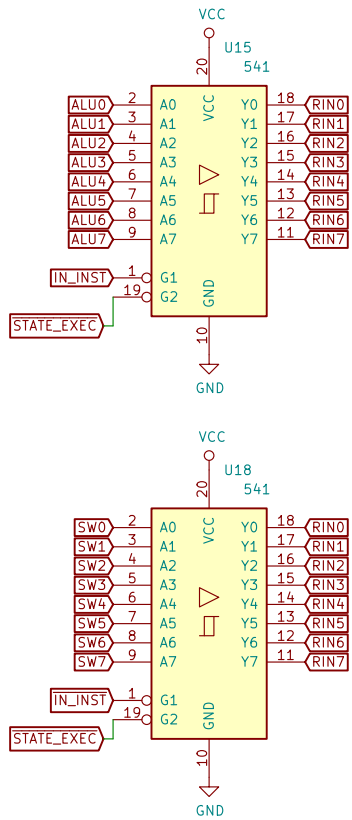


Two phase clock generation.  
SC advances the state machine.  
WS is the write strobe for writing registers.

Sheet: /Clock/		File: clock.sch	
<b>Title:</b>			
Size: A4	Date:	Rev:	
KiCad E.D.A. kicad (5.1.2-1)-1			Id: 4/12



DECD is asserted to check for zero.

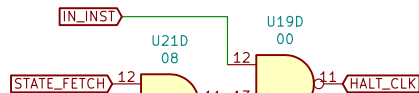
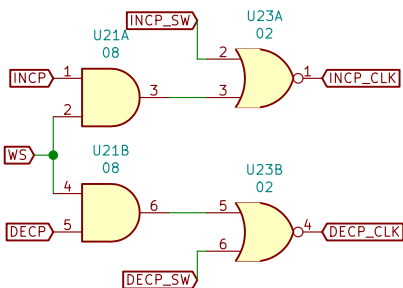
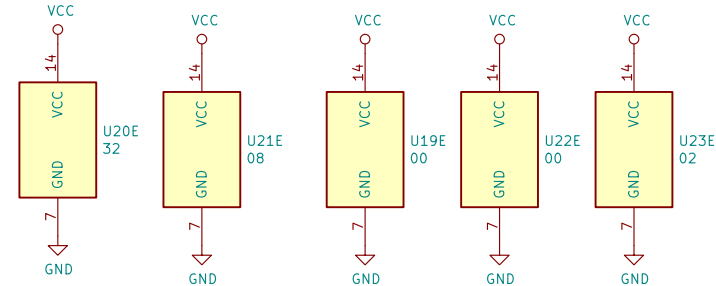
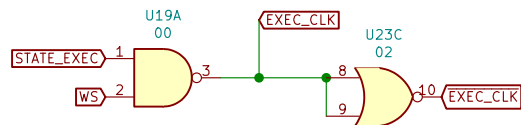
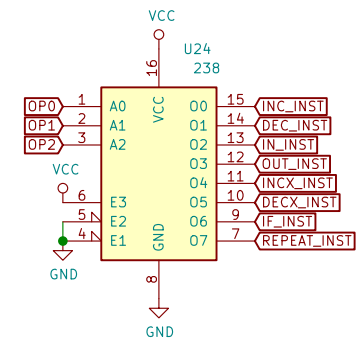


Sheet: /ALU/  
File: alu.sch

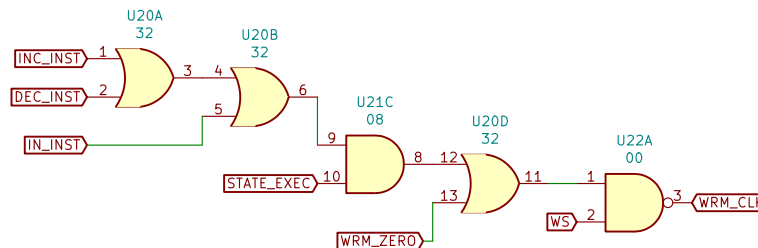
**Title:**

Size: A4 Date:  
KiCad E.D.A. kicad (5.1.2-1)-1

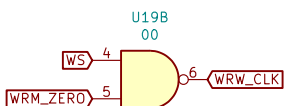
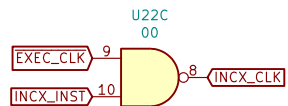
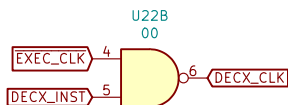
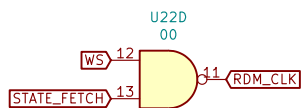
**Rev:**  
Id: 5/12



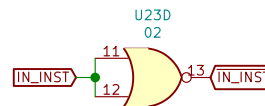
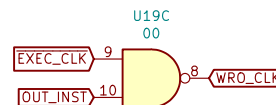
For input instructions, we stop the clock during the fetch phase to allow the user to change the input switches.



We write to memory on INC/DEC/IN instructions during STATE\_EXEC. We also write to memory during STATE\_EXEC if a new watermark has been set.



Update the watermark when writing a zero to RAM.



×

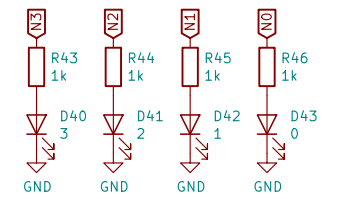
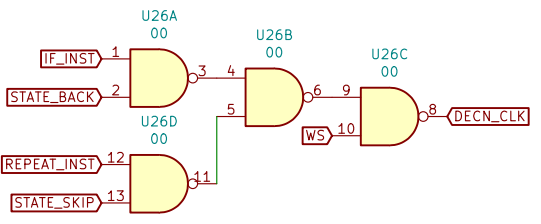
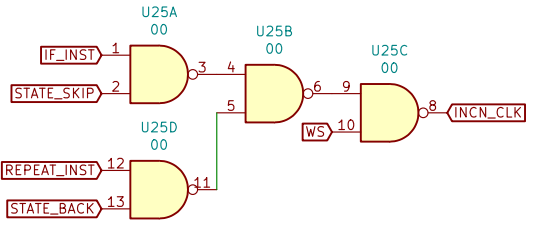
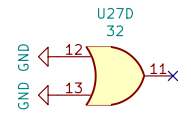
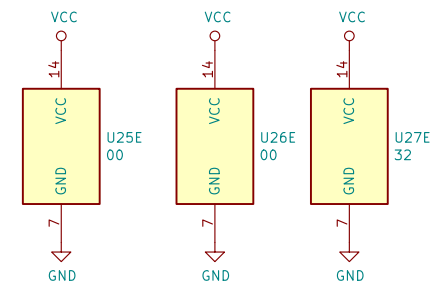
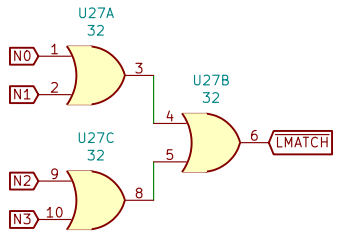
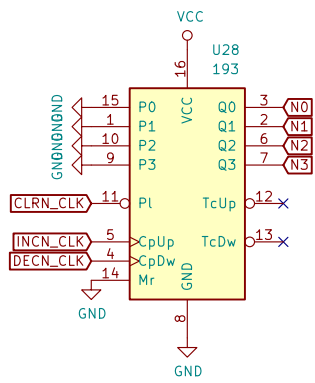
Misc control logic.  
Some of this spills into the state machine schematic.

Sheet: /Control/  
File: control.sch

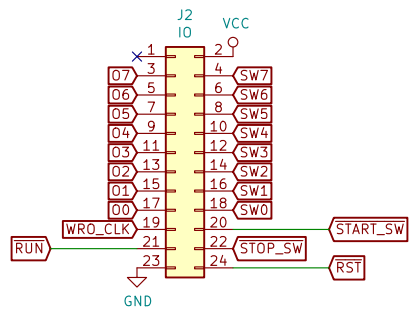
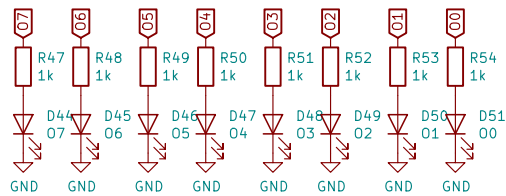
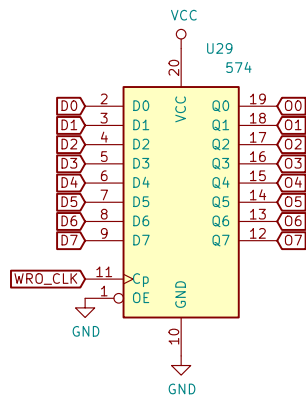
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Size: A4  
KiCad E.D.A. kicad (5.1.2-1)-1

Date:  
Rev:  
Id: 6/12



Sheet: /Label Register/ File: label.sch		
<b>Title:</b>		
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 7/12



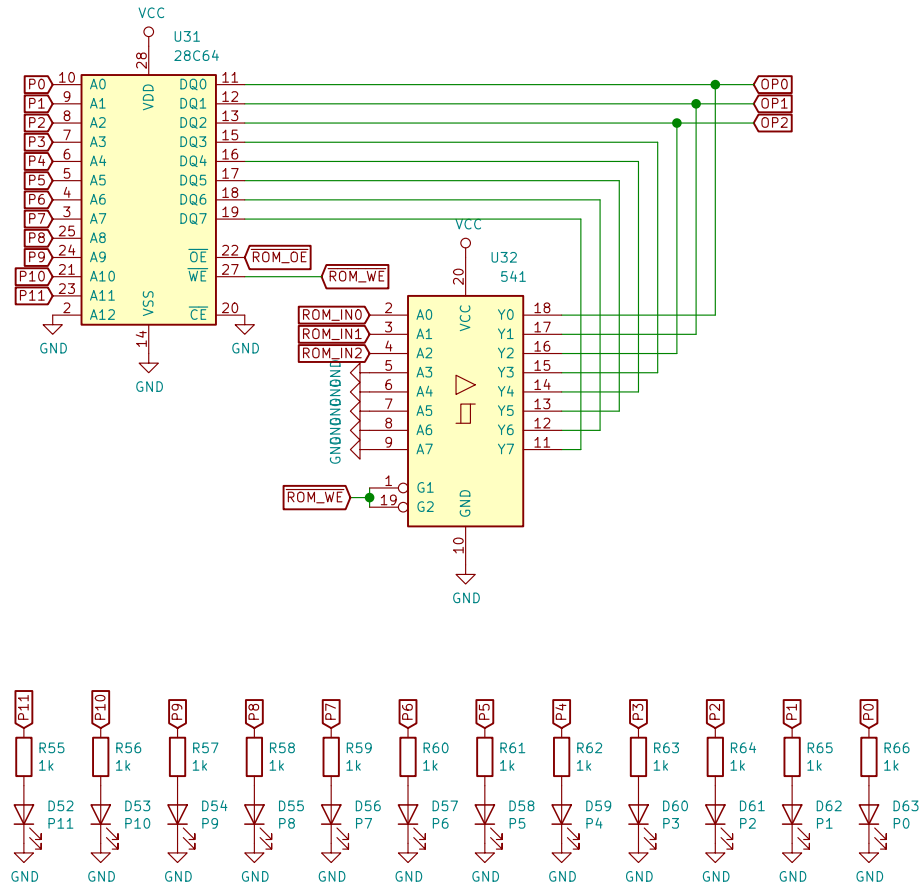
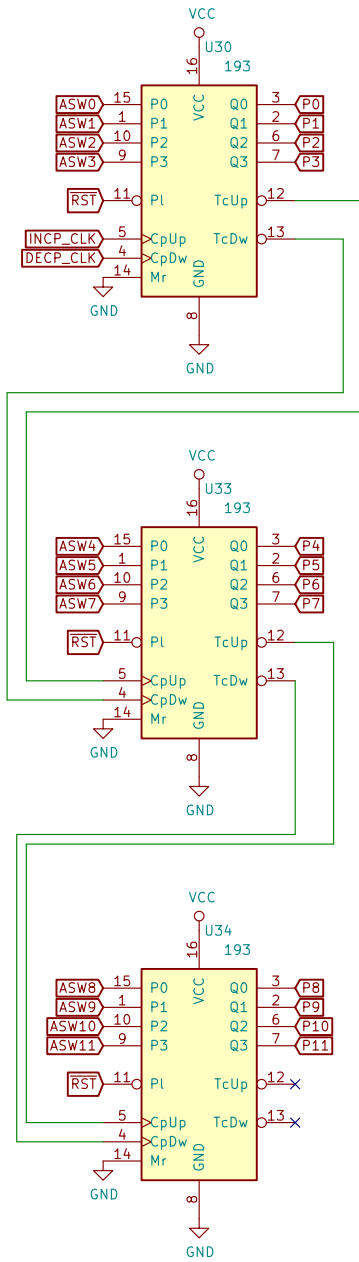
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File: output.sch

**Title:**

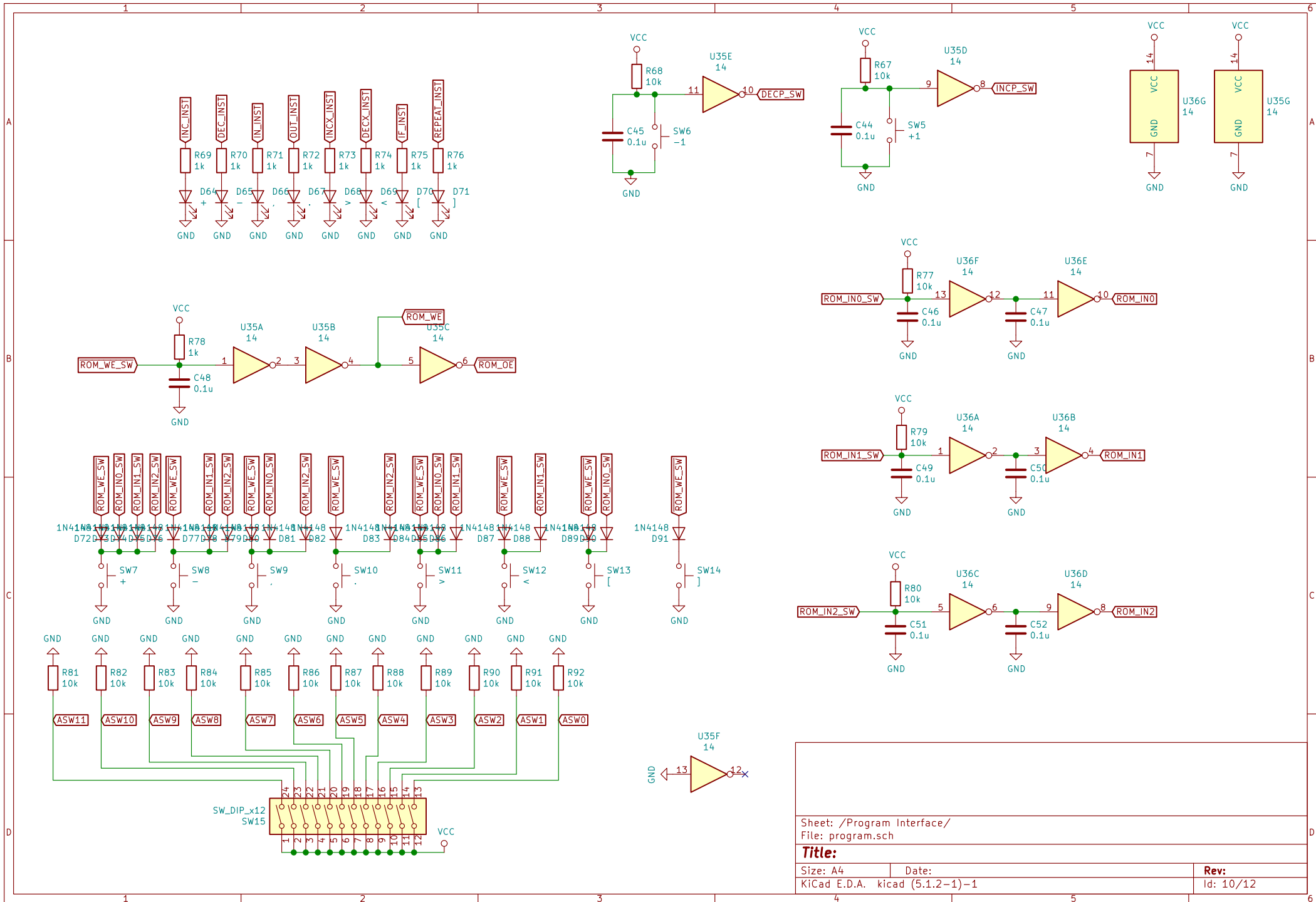
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Date:  
Rev: 8/12

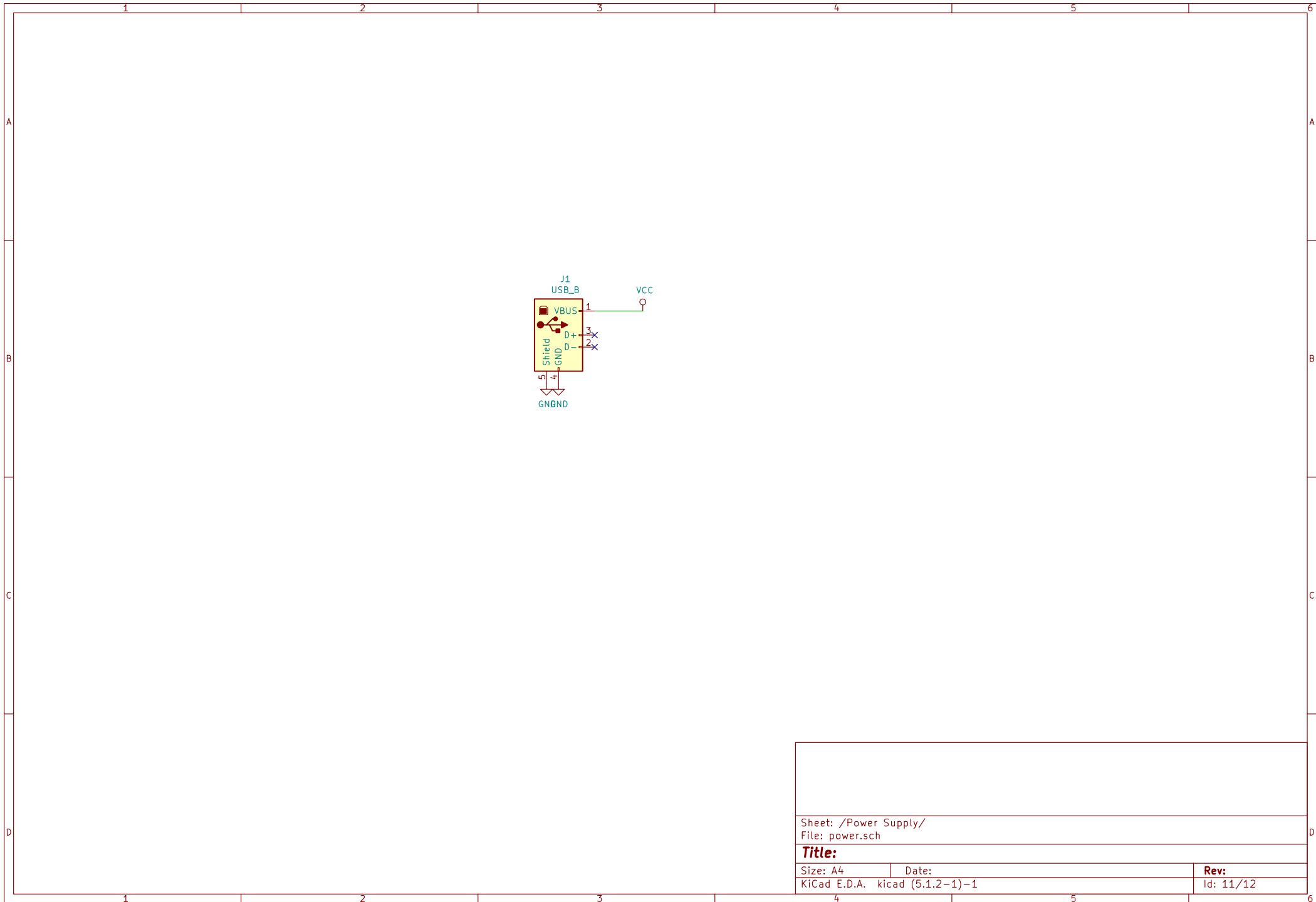




Sheet: /ROM/	
File: rom.sch	
<b>Title:</b>	
Size: A4	Date:
KiCad E.D.A. kicad (5.1.2-1)-1	
<b>Rev:</b>	
Id: 9/12	



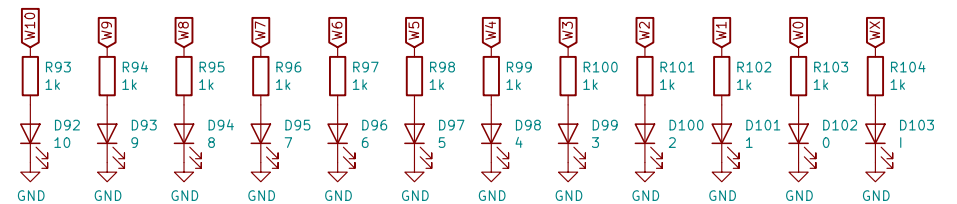
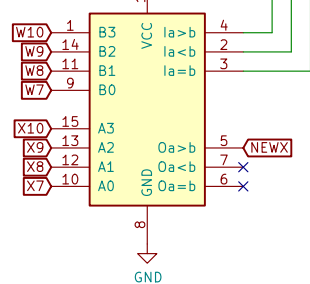
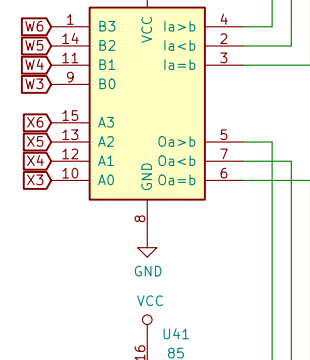
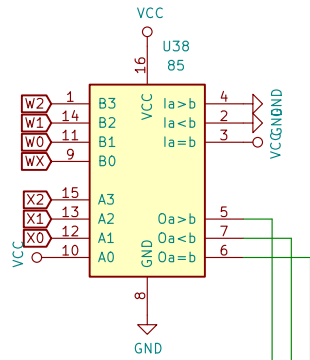
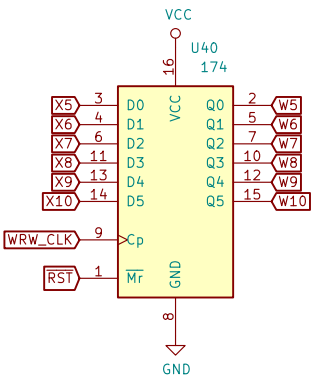
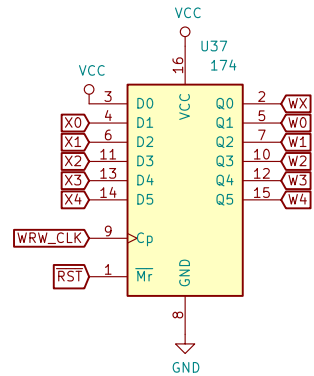
Sheet: /Program Interface/ File: program.sch	
<b>Title:</b>	
Size: A4	Date:
KiCad E.D.A. kicad (5.1.2-1)-1	Rev:
	Id: 10/12



Sheet: /Power Supply/  
File: power.sch

**Title:**

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 11/12



The W register and comparator logic is used to track when a new high watermark has been set when accessing memory. This allows us to set the value to zero, making it appear as if all cells are initialized to zero.

Sheet: /Watermark/  
File: watermark.sch

**Title:**

Size: A4  
KiCad E.D.A. kicad (5.1.2-1)-1

Date:  
Rev:  
Id: 12/12